

# Claims

- [c1] A bipolar transistor, comprising:
  - a collector layer;
  - an intrinsic base layer overlying said collector layer;
  - a low-capacitance region laterally adjacent to said collector layer including at least one of a dielectric region and a void disposed in an undercut underlying said intrinsic base layer;
  - an emitter layer overlying said intrinsic base layer; and
  - a raised extrinsic base layer overlying said intrinsic base layer.
- [c2] A bipolar transistor as claimed in claim 1, wherein said dielectric region includes a void underlying said intrinsic base layer.
- [c3] A bipolar transistor as claimed in claim 1, wherein said low-capacitance region includes at least one of a void and a solid dielectric region contacting said collector layer.
- [c4] A bipolar transistor as claimed in claim 3, wherein said intrinsic base layer is surrounded by said dielectric region.

- [c5] A bipolar transistor as claimed in claim 1, wherein said raised extrinsic base layer is self-aligned to said emitter layer.
- [c6] A bipolar transistor as claimed in claim 5, wherein said raised extrinsic base layer is spaced from said emitter layer by a first spacer having a sidewall wholly in contact with said raised extrinsic base layer and a second spacer overlying said first spacer, said second spacer having a sidewall wholly in contact with said emitter layer.
- [c7] A bipolar transistor as claimed in claim 1, wherein said collector layer has a dopant concentration of about  $10^{20} \text{ cm}^{-3}$ .
- [c8] A bipolar transistor as claimed in claim 1, further comprising a subcollector disposed below said collector layer, and a trench isolation region surrounding peripheral edges of said subcollector.
- [c9] A bipolar transistor as claimed in claim 1, wherein said intrinsic base layer includes a layer of a single-crystal semiconductor material which forms a heterojunction with a material of at least one of said emitter layer and said collector layer.
- [c10] A bipolar transistor as claimed in claim 1, wherein said

single-crystal semiconductor material layer included in said intrinsic base layer includes silicon germanium.

- [c11] A method of making a bipolar transistor, comprising:  
forming a structure including an intrinsic base layer overlying a collector layer, and a low capacitance region including a dielectric region disposed in an undercut underlying said intrinsic base layer and laterally adjacent to said collector layer; and  
forming an emitter layer and a raised extrinsic base layer overlying said intrinsic base layer.
- [c12] A method of making a bipolar transistor as claimed in claim 11, wherein said dielectric region includes a void underlying said intrinsic base layer.
- [c13] A method of making a bipolar transistor as claimed in claim 11, wherein said low-capacitance region includes at least one of a void and a solid dielectric region contacting said collector layer.
- [c14] A method of making a bipolar transistor as claimed in claim 11, wherein said collector layer is doped to a final dopant concentration after said intrinsic base layer is formed.
- [c15] A method of making a bipolar transistor as claimed in claim 14, wherein said intrinsic base layer is formed over

said collector layer and said collector layer is doped to said final dopant concentration by forming said undercut below said intrinsic base layer and supplying a dopant to said collector layer through said undercut.

[c16] A method of making a bipolar transistor as claimed in claim 15, wherein said dopant is supplied to said collector layer in gas phase.

[c17] A method of making a bipolar transistor as claimed in claim 15, wherein said low capacitance region extends above a top surface of said collector layer, wherein at least a portion of said raised extrinsic base layer is formed over said low capacitance region.

[c18] A method of making a bipolar transistor as claimed in claim 17, wherein said structure further includes a sub-collector disposed below said collector layer, and a trench isolation region surrounding peripheral edges of said subcollector.

[c19] A method of making a bipolar transistor as claimed in claim 11, wherein said intrinsic base layer includes a layer of a single-crystal semiconductor which forms a heterojunction with at least one of said emitter layer and said collector layer.

[c20] A method of making a bipolar transistor as claimed in

claim 11, wherein said single-crystal semiconductor material layer of said intrinsic base layer includes silicon germanium.